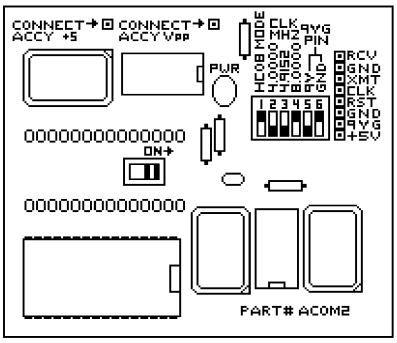
# USING THE ACOM2 ASYCHRONOUS COMMUNICATION ADAPTER WITH MOTOROLA MICROCONTROLLERS

The ACOM2 ayschronous communication adapter allows the EPROM+ system to address multiple microcontroller technology families manufactured by Motorola (Freescale). The ACOM2 provides a complete asychronous communication subsystem plus the required interface voltages and clock signals necessary to establish communication with each technology family. The technology families include the 68HC11, 68HC08/908 and 68HC05. Each family is unique in the requirements to attach and establish communication. This document covers each family in a separate section which allows you to reference only the material specific to your application. The following information describes the general features and operation of the ACOM2 adapter. Please read this before installing and using the ACOM2. **NOTE**: See the last pages of this document for microcontroller physical connection illustrations.

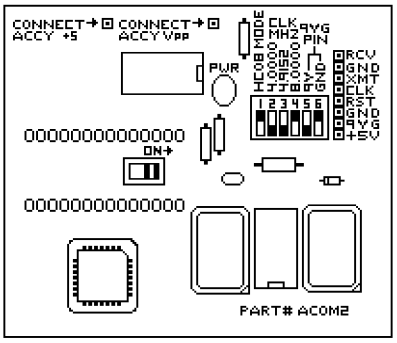
## INSTALLING THE ACOM2 ADAPTER

Before installing the ACOM2 adapter, be sure that the programming unit DIP SWITCH is set correctly (3 and 5 ON, all others OFF) as the switch cannot be accessed after the adapter is installed. The ACOM2 adapter has a 28 pin base and is therefore installed in the AR-32A programming unit left justified. To install the adapter, lift the ZIF socket release handle on the 32 pin socket to about 45 degrees. This will release the socket mechanism. Be sure the adapter is fully left justified and insert the pins into the socket. Release the handle to lock the adapter in place. The ACOM2 adapter requires power from the programming unit ACCESSORY CONNECTOR. Be sure the adapter power switch is OFF (left position). Attach the +5V (ORANGE) wire to the +5 pin on the accessory connector. Attach the Vpp (YELLOW) wire to the Vpp pin on the accessory connector. The adapter is now ready for use.

## CONFIGURING AND USING THE ACOM2 ADAPTER




The ACOM2 adapter is configured using the 6 position dip switch (see illustration). This switch allows the setting of three parameters; processor clock speed, 9VG pin level and HC08 configuration mode. **NOTE 1:** The system software will automatically display the correct ACOM2 switch setting when a supported device is selected. **NOTE 2:** There are two versions of the ACOM2. The top illustration shows the REV B board. The REV C/D adapter (lower illustration) uses a 28 pin PLCC communication chip and generates a 2MHZ clock. (NOTE: A REV B adapter may be upgraded to the same functionality as a REV C/D board.)




### SWITCH 1 - HC08 MODE

Switch 1 sets the adapter for full duplex (transmit and receive on separate lines) or half duplex (transmit and receive on the same (shared) line). The 68HC08/908 processor family uses a half duplex protocol to comminicate with the processor in what Motorola calls MONITOR MODE. Setting switch 1 to ON connects the XMT and RCV line together through a circuit which allows the signals to coexist on a single line. This is the RCV (receive) line and it must be used to connect to the HC08/908 target processor.

### SWITCHES 2, 3 and 4 - CLK MHZ

Switches 2, 3 and 4 select the processor clock frequency. Setting a switch to ON will route the selected clock frequency to the CLK pin on the target connector. Each family requires a different processor clock frequency to establish the correct communication baud rate (HC05 - 4.0000 MHZ | HC08/908AS - 4.9152 MHZ | HC08/908AZ - 2.0000 MHZ | HC11 - 8.0000 MHZ). Only set one switch at a time to the ON position. **NOTE:** The clock frequency will be 2.000 MHZ if SW2, 3 and 4 are all open for a REV C/D adapter.

### SWITCHES 5 and 6 - 9VG PIN

Switches 5 and 6 select the voltage level at the target connector 9VG PIN. The 9VG pin is so named for the two voltage levels; 9V (9 volts) or G (ground). In most cases the HC05 and HC08/908 families require that 9 volts DC be present on the IRQ pin before the processor will enter a communication or monitor mode. The HC11 family does not require the elevated voltage to enter the bootstrap communication mode. Set switch 5 ON and switch 6 OFF to set the 9VG pin to 9 volts. Set switch 6 ON and switch 5 OFF to set the 9VG pin to GND.

### ADAPTER POWER SWITCH

The ACOM2 adapter includes a slide switch which applies power to both the adapter and the target connector. There is an LED marked PWR which illuminates when power is on. The power switch is provided to allow the adapter to be connected to the target without the possibility of damage. Once the adapter is connected to the target, set the power switch to ON.

# USING THE ACOM2 ADAPTER WITH THE MOTOROLA 68HC11 PROCESSOR FAMILY

The ACOM2 provides the EPROM+ system with a complete asychronous communication subsystem. This subsystem allows the EPROM+ to support the Motorola 68HC11 family of microcontrollers via the on-chip serial communication interface in conjunction with the processors “BOOTSTRAP” mode.

## ABOUT THE 68HC11 “BOOTSTRAP” MODE

All members of the Motorola 68HC11 family of microcontroller include a special mode of chip operation called “BOOTSTRAP” mode. BOOTSTRAP mode allows any program to be uploaded, using the 68HC11 serial communication interface, into the internal RAM memory of the 68HC11 and then executed. The EPROM+ system uses BOOTSTRAP mode to initially upload a communication program into the 68HC11. The communication program then establishes a link with the EPROM+ system whereby the internal EPROM, EEPROM and I/O become accessable. The 68HC11 processor must be forced to enter “BOOTSTRAP” mode after a processor reset or the initial application of power. Specific conditions must exist for the processor to enter BOOTSTRAP mode. These are:

**1. The processor MODE pins (MODA and MODB) must both be at logic 0 or ground when the processor leaves reset or power is applied.**

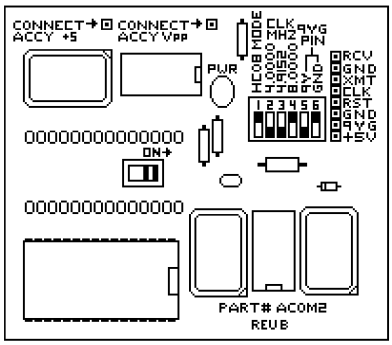
**2. The processor must be operating at 8 MHZ. This may be from an externally attached crystal or a supplied frequency source attached to the processor EXTAL pin.**

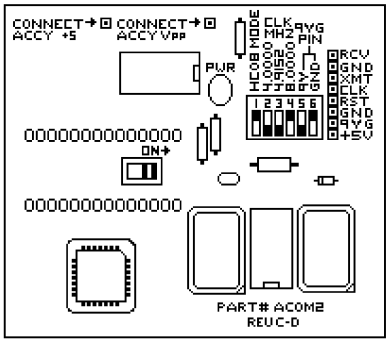
**3. The RxD and TxD pins must be unencumbered by circuitry and and be free to attach to the proper pins on the ACOM2 adapter.**

**NOTE:** If any of the initial conditions listed above are not valid when the 68HC11 processor leaves reset, the processor will not enter BOOTSTRAP mode and the communication program cannot be uploaded.

## CONNECTING THE ACOM2 ADAPTER TO THE 68HC11 TARGET PROCESSOR

The ACOM2 adapter includes all necessary circuitry to communicate with a 68HC11 processor. Each pin on the adapter connector is described regarding its connection to the target processor. Read the descriptions below and connect the proper adapter pins to the correct pins on the 68HC11 target processor. Note that no processor pin numbers are referenced as the actual physical target processor package must be used to determine the true pin number. This information may be obtained by examining the processor data sheet or the diagrams at the end of this document..




**GND** - These pins are connected to the EPROM+ system ground and at least one must be connected to the 68HC11 ground or Vss pin. There are three pins provided if it is necessary to force the MODA or MODB processor pins to 0.

**RCV** - This is the input to the serial data RECEIVER on the ASYNC adapter. It must be connected to the TxD (transmit) pin on the processor.

**XMT** - This is the output from the serial data TRANSMITTER on the ASYNC adapter. It must be connected to the RxD (receive) pin on the processor.

**CLK** - This is an 8 MHZ source which may be connected to the processor EXTAL pin if needed. Set SW2 on the 6 position dip switch to ON for 8 MHZ.

**RST** - This pin is available to manually reset the processor before the BOOTSTRAP upload begins. It may be connected to the processor RESET line if necessary. It is not necessary to connect this pin if the processor is started from a “power off” state as the “power on” sequence will automatically perform a processor reset.

**9VG** - This pin must be set to GND (SW6 ON) if it is to be used as a ground connection on the HC11 processor.

**+5V** - This pin is a source of 5 volt power. It may be used to power the processor in “stand-alone” operation but may not have sufficient current capability to power a complete circuit assembly. Current capacity is approximately 100mA.

**ACOM2 POWER SWITCH**

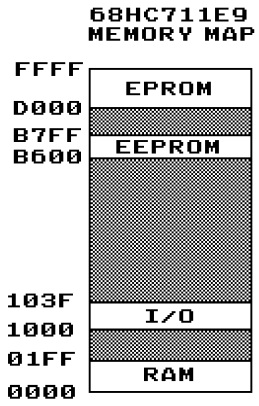
Before connecting the HC11 processor to the ACOM2, be sure the POWER SWITCH is set to OFF (left). Once the target processor is attached to the ACOM2 adapter, you may apply power to both the ACOM2 adapter and the target processor by setting the POWER SWITCH to ON (right). The PWR LED will light when power is applied. This procedure allows the target processor to be safely connected to the adapter before any power is applied.

# INITIATING COMMUNICATIONS WITH THE TARGET PROCESSOR

Before initiating communications with the target 68HC11 processor, the processor must have power applied and have successfully entered “BOOTSTRAP” mode from reset. If you have connected the adapter RST pin to the processor RESET pin, the EPROM+ software will automatically generate a processor reset before performing the program upload. The communicaton program upload is initiated using the “Z” command (DEVICE OPTIONS). Press “Z”. You will see three options. Press “1”. This will automatically read the communication program into the system buffer and perform the upload operation. You will see the following messages: “BOOTSTRAP UPLOAD IN PROGRESS...”, “BUFFER UPLOAD COMPLETE”, “COMMUNICATION VERIFIED”. The system indicates the current operation. The last message (COMMUNICATION VERIFIED) must be displayed in order for the EPROM+ to communicate with the target processor. If this message is not displayed, the communication program is not active and the target processor may not be accessed. If the “COMMUNICATION VERIFIED” message is not displayed, verify that the conditions listed under “CONNECTING THE ACOM2 ADAPTER TO THE 68HC11 TARGET PROCESSOR” are correct. NOTE: If you have not connected the adapter RST pin to the target processor the system will display: “WARNING! CONNECTION NOT CONFIRMED FROM TARGET PROCESSOR AFTER RESET”. This message indicates that the EPROM+ system did not receive a confirmation from the target processor after the EPROM+ system initiated a reset. This is a normal message if you do not have the RST pin connected. After the processor is reset in “BOOTSTRAP” mode, it transmits a single response called a “BREAK”. The EPROM+ software checks for the “BREAK” response after the reset. If you manually reset the processor by applying power, the “BREAK” response occurs before the EPROM+ is ready. This in no way causes a problem and the program upload progresses normally.

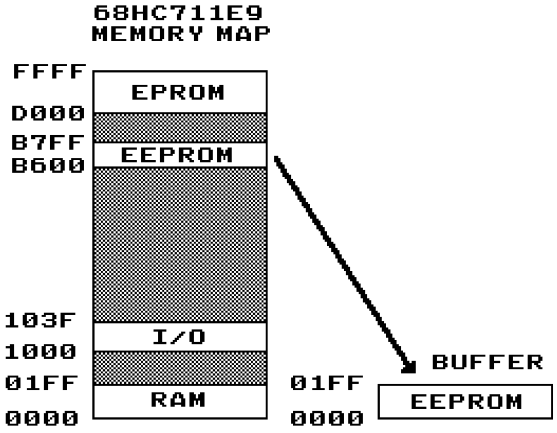
# ACCESSING THE INTERNAL MEMORY OF THE 68HC11

Once communication has been established with the target processor, all EPROM+ software functions are available to access the internal memory of the 68HC11. The EPROM+ software remains in communication with the target processor until you exit the program, change the device type or power down the target. The internal memory of the 68HC11 depends on the series of part with which you are working. For purposes of illustration, this example will use the 68HC711E9. The 68HC711E9 actually has three accessable areas of memory. These are RAM, EEPROM and EPROM (see first figure). While the communication program is active it occupies the lower 256 bytes of RAM (0-FF). Note that the EEPROM exists between addresses B600 and B7FF (512 bytes) and EPROM exists between D000 and FFFF (12K bytes). The EPROM+ sofware allows you to easily work with the EEPROM or EPROM as if it were the only memory in the part. This means, for example, that you may work with the EEPROM as if it were an individual memory part of 512 bytes with a starting address of 0 and an ending address of 1FF (see second figure). This is much easier than working with the memory map offset of B600 to B7FF. The same is true for the EPROM. The software automatically remaps the EEPROM such that if you read the part, the EEPROM data will appear in the buffer from 0 to 1FF. The system defaults to EEPROM for the area of the memory map which will be accessed if the part contains EEPROM. If the part only contains EPROM or RAM, the system will default to EPROM first, then RAM.




# CHANGING THE AREA OF ACCESS

The software allows you to change the memory area accessed by the system. This is accomplished from the “O”ptions selection from the first set of “UPLOAD (BOOTSTRAP) PROGRAM TO DEVICE” options. Press “O”. You are presented with three memory access areas. Choose the area you wish to remap to buffer address 0. Note: These options are always displayed even if the part does not have the memory physically implemented. If you attempt to access EEPROM in a part within which the memory does not exist, you will be notified with an error message. Once the desired area is selected, the software automatically uses the proper programming algorithm. The current area will remain active until it is changed or the system is shut down.



# FEATURES FOR ADVANCED USERS

The standard access provided for EEPROM/EPROM reading and programing are more than adequate for typical maintenance and service applications. The software, however, has features for the technically advanced user who has interest in product development or testing of existing systems. The following features are provided:

1. Upload (bootstrap) any program you wish from the system buffer into the 68HC11.
2. Access the entire 64K address range of the processor including all memory and I/O registers.
3. Select the programming algorithm to be used while accessing the 64K range.
4. Transfer control to a "USER PROGRAM" and display a returned "BYTE" value.

Each feature is described below.

## 1. Upload (bootstrap) any program into the 68HC11

This feature is accessed from the initial "Z" (DEVICE OPTIONS) option list. In addition to Option 1, which uploads the communication program into the 68HC11, Option 2 will upload the first 256 bytes of the system buffer into the processor and then transfer control to the program at address 0. Option 3 performs the same function except you have the option of specifying the exact number of bytes to upload. This value may be from 0 to FFFF. You will be prompted for the buffer ending address at which the upload will cease.

## 2. Access the entire 64K address range

This feature is accessed from the same option selections used to choose the memory access area. Choose Option 3 (ENTIRE 64K ADDRESS RANGE). This causes the buffer addresses to exactly match the device addresses. For example if you perform a ZONE READ (Command 3 - Option 2) at device address B600 through B7FF into the buffer at address B600 you will read the internal EEPROM of a 68HC711E9 and place the information into the buffer at exactly the same addresses at which it exists in the processor. This access mode allows you to view and modify any location you choose within the processor. Use caution as this access mode also allows you access to the first 256 (0-FF) bytes of RAM where the communications program resides.

## 3. Select the programming algorithm to be used while accessing the 64K range

This feature is accessed as an option under "MEMORY ACCESS OPTIONS". Note that the 64K range must be selected as the current access option before the programming algorithm may be changed. Once the "PROGRAMMING ALGORITHM FOR 64K RANGE" is displayed, choose the algorithm which is to be used by the system for programming. With the selections available, you may perform direct RAM and I/O writes, EEPROM writes or EPROM writes. Note that Vpp (12.75V) must be applied to the processor Vpp pin before the internal EPROM may be programmed. You may use this feature to change the setting of the CONFIGURATION register which is implemented with EEPROM cells.

## 4. Transfer control to a "USER PROGRAM" and display a returned "BYTE" value

This feature is accessed as an option under "PROGRAMMING ALGORITHM FOR 64K RANGE". It is specifically intended for the testing of small user programs loaded into RAM, EEPROM or EPROM. The program to be executed (user program) must be loaded into the processors physical memory. This may be accomplished using the buffer "WRITE" command which writes a block of data from anywhere in the buffer to anywhere in the device. Once the program in transferred to the 68HC11 memory, enter the starting address for the program at the prompt and press <ENTER>. Control will be transferred to the program at the specified address. The EPROM+ software will now wait for a byte to be returned from the user program. If you wish to view a returned byte from the user program it must be loaded into Accumulator A (ACCA) of the 68HC11. A "JUMP TO SUBROUTINE" (JSR) must then be executed to fixed address $0005. This will cause the byte in ACCA to be transmitted via the communication program back to the EPROM+ software where it is displayed to the operator. This "RETURN BYTE" capability allows you to monitor data or status from your program which may be used for testing or debugging. Note that ACCA is destroyed by the transmit subroutine. To return control to the EPROM+ software from the user program you may execute an extended (16 bit) jump (JMP) to address $0008. This will allow you to again access the 64K address range after your program is done executing. This is useful if your program has left data or status information in memory that you wish to examine. Note: You may terminate the "RETURN BYTE" monitoring loop of the EPROM+ software while the user program is executing by pressing ESC.

**NOTES:** The stack is located at address $00FF. There are about 8 bytes of free stack space after the communication program. If your program requires more space then the stacked should be moved. The communication program occupies the first 256 bytes including the stack. If you overwrite this area communications will be lost and the communication program will need to be reloaded. The communication program uses the 68HC11 SCI.

# INTERFACING AND COMMUNICATING WITH THE 68HC05/705 MICROCONTROLLER FAMILY

This document provides information necessary to interface the Andromeda Research EPROM+ programming system to certain members of the Motorola 68HC05/705 microcontroller family. The interface is accomplished using the ACOM2 adapter by uploading a small communication program into the RAM area of the 68HC05 device. Once uploaded, the program establishes a communication link between the 68HC05 and the EPROM+ system. The communication program allows the EPROM+ system access to the internal EPROM, EEPROM, ROM, RAM or I/O area of the part.

## ABOUT THE 68HC05 FAMILY

The 68HC05 microcontroller family is composed of more than 100 different members (parts). These include limited function devices in small packages intended for simple applications plus complex devices intended for more sophisticated products. All family members use the same basic processor core and differ only in the amount of memory (ROM, EPROM, EEPROM and RAM) plus peripheral options such as I/O ports, timers, counters, pulse width modulators, comparitors, etc. **NOTE:** Motorola identifies parts containing user programmable EPROM with 705 in the part number as opposed to 05. For example, the 68HC705C8 microcontroller has user programmable EPROM where the 68HC05B16 has factory programmed mask rom. This document does not address the specific technical attributes of any member of the 68HC05 family. If you require information regarding a specific part it may be obtained from the Freescale website (www.freescale.com). Motorola spun off their microcontroller division and changed the name to Freescale. **NOTE:** This document uses the $ which is Motorola's standard syntax for represending hexadecimal numbers. Example: $100 represents 100 hexadecimal.

## COMPATIBLE FAMILY MEMBERS

The EPROM+ system is compatible with members of the 68HC05 family which support the following internal architectural components and chip features:

1 - SCI port (Serial Communication Interface)
2 - 176 bytes of internal RAM mapped at $0050.
3 - Load program into RAM and execute function (binary image program only loaded at $0050).

**NOTE:** Some members of the 68HC05 family do not support the function which allows a binary program to be loaded into the RAM area at $0050 and executed. If this function is not supported, the communication program upload will fail. An example part which does not support the binary upload function is the 68HC705B5.

## SELECTING THE PART

The EPROM+ system requires that you choose a specific part number depending on the task you wish to perform. Due to the limited RAM in a 68HC05 device, it is not possible to provide a single communication program which allows programming of both the EEPROM and EPROM. To this end, there are two communication programs, one contains the algorithm which allows you to read and program the on-chip EEPROM area, the other contains the algorithm which allows you to read and program the EPROM area. The correct program is uploaded depending on the part number you choose. There are multiple device specific part numbers available plus two generic. Two device specific part number examples are the 68HC05B16 (EEPROM) and the 68HC705C8 (EPROM). The two generic part numbers are the 68HC05EE (EEPROM) and the 68HC705EP (EPROM). In the event that you are working with a part which is not listed in the DEVICE SELECTION TABLE, you may choose the corresponding generic number depending on the task you wish to perform (EEPROM or EPROM access and programming).

## CONNECTING THE ACOM2 ADAPTER TO THE 68HC05 TARGET PROCESSOR

In order for the 68HC05 microcontroller to accept and successfully upload the communication program the following conditions must exist:

1. Connections to the part must include power (Vdd and Vss), proper logic levels (+5 or GND) applied to specified pins plus, in some cases, 9 volts DC applied to the IRQ pin. This differs depending on the part. Reference the diagrams at the end of this document for the proper pin connections. If any of these conditions are not met, the part will not enter the bootstrap or upload mode following reset.
2. Set SW2 to the ON position to route 4 MHZ to the adapter CLK pin and connect this signal to the CLOCK or EXTAL input on the target processor.
4. Connect the ACOM2 to the RST (reset), XMT (transmit) and RCV (receive) pins on the 68HC05 target processor.
5. If the 68HC05 requires 9 volts on the IRQ pin, set SW5 ON and SW6 OFF. Connect the 9VG pin to the IRQ pin on the target processor.
6. Set the ACOM2 power switch to ON. This will apply power to the ACOM2 and the target processor. You are now ready to proceed with the program upload.

## UNDERSTANDING THE EEPROM AND EPROM DIFFERENCES

**EEPROM MODE (68HC05EE)** - Choosing the 68HC05EE will upload the communication program which allows reading and programming of the EEPROM area of a 68HC05. In the normal 64K address range ($0-$FFFF) of a 68HC05 part with on-chip EEPROM, the EEPROM will be mapped between $100 and $1FF (256 bytes). The EPROM+ software makes this 256 byte block of memory appear to begin at address $0 and end at address $FF. This is done to allow you to work with the EEPROM area within the part unencumbered by the fixed offset of $100. When you instruct the system to read, the EEPROM area will be loaded into the system buffer beginning at 0 and ending at FF. Conversly, when you instruct the system to program, the buffer area between 0 and FF will automatically be placed into the part between $100 and $1FF.

**EPROM MODE (68HC705EP)** - Choosing the 68HC705EP will upload the communication program which allows reading and programming of any EPROM area of a 68HC705. You are actually permitted access to the entire 64K ($0-$FFFF) address range as there is no consistent block of memory allocated only to EPROM in the 68HC05 family. When accessing a 68HC705 or 68HC05 part, you may examine any address within the 64K range. In order to program the EPROM area you must apply the required external programming voltage to the Vpp pin on the processor. For the 68HC705C8 device, the is 14.75 volts. The buffer editor "W" (write) command must be used to write the data from the buffer into the 68HC705 over the desired address range.

**STANDARD MEMORY READ/WRITE**

While in the EPROM MODE (68HC705EP), you may also perform standard memory read and write operations. These are the same as processor LOAD and STORE instructions. This allows you to exercise I/O ports or examine and change any address within the 64K range. To select this option press "Z" at the "SELECT COMMAND" prompt. Select "O" for options then press "3" to choose the entire 64K address range. Press "O" for options and choose "1" for memory write. Press "ESC" twice to return to the COMMAND PROMPT. You may now use any main or editor command to read or write the device. **NOTE:** If you wish to work with the EEPROM area (68HC05EE) while in the 64K mode, use the previous option selections except choose "2" "EEPROM ALGORITHM" instead of "1" (memory write).

**UPLOAD SEQUENCE AND OPTIONS**

Before any operation can be performed on the 68HC05/705 the appropriate communication program must first be uploaded. To achieve a successful upload, the conditions listed under REQUIREMENTS FOR SUCCESSFUL UPLOAD AND COMMUNICATION must exist. Once these conditions are met, perform the following steps:

**1 - From the COMMAND PROMPT press "Z" (device options)**
**2 - Press "1 - UPLOAD 68HCXX COMMUNICATION PROGRAM"**
You will see: "BOOTSTRAP UPLOAD IN PROGRESS..."
**3 - When the upload is finished your will see "* BUFFER UPLOAD COMPLETE *"**
**4 - The EPROM+ software will now attempt to confirm that communication can be established with the 68HC05.**
If communications is established you will see (COMMUNICATION VERIFIED) displayed directly below * BUFFER UPLOAD COMPLETE *. *Watch for it.* If the COMMUNICATION VERIFIED message is not displayed, communication with the 68HC05 part has not been established and no system commands will function. If this happens, you must determine the cause and correct the problem. Note: The * BUFFER UPLOAD COMPLETE * and (COMMUNICATION VERIFIED) messages are displayed for a short period and then automatically erased.

**ADDITIONAL CONSIDERATIONS**

1. The communication program will continue to run in the 68HC05 until power is removed or the processor is reset. Remember that if you temporarily remove power from the part, you must again upload the communication program.
2. The communication program loads and runs in the 68HC05 RAM area beginning at $0050. If you use the memory write function of the program to alter any addresses in this area, you will corrupt the program and communication will stop.

**UPLOAD ANY TEST PROGRAM INTO THE 68HC05 RAM AREA**

If you have the technical skill to create your own test program and wish to upload it into the 68HC05 part, this can be accomplished by pressing "Z" and choosing option 2 or 3. Create your program with the ORIGIN at $51. Load the program into the buffer and then transfer it ("T" command) to buffer address 0001. Count the total number of bytes plus 1 and place this number (in binary) at buffer address 0 (byte count). Upload your program. **NOTE:** The binary image structure of the program follows:
$50 - byte count of program including this byte (if you have a five byte program this value will be $06)
$51 - First byte of program (execution starts here)
$52 through $FF (remaining bytes in 176 byte area)
**NOTE**: When the processor starts from reset, it places the STACK at $FF. Be aware of this as it can limit the available space for your program depending on the use of subroutines.

# USING THE ACOM2 ADAPTER WITH THE MOTOROLA 68HC08/908 MICROCONTROLLER FAMILY

This document provides information necessary to interface the Andromeda Research EPROM+ programming system to certain members of the Motorola 68HC08/908 microcontroller family. The interface is accomplished using the ACOM2 adapter by invoking functions provided by the internal Monitor program. The Monitor is a small program included in some members of this microcontroller family which allows access to the 64K address space. Through use of the monitor functions, the EPROM+ system software allows you to read any memory location within the 64K address space, plus program both the EEPROM and RAM.

## ABOUT THE 68HC08/908 AND THE MONITOR MODE

Motorola created the monitor to provide a simple interface to the internal functions of the HC08/908 architecture. It occupies part of the microcontroller ROM area for the specific purpose of low level rudamentary testing. Monitor communications occur in half-duplex with character echo over a single pin on the processor package. Although this provides a simple interface connection, it does not use the internal communication functions of the part which results in limited speed and reduced communication integrity.

## COMPATIBLE FAMILY MEMBERS

The EPROM+ system software implements the published communication protocol as defined by Motorola. This protocol, in most cases, has proven successful with the 68HC08/908AS and AZ family members. Due to requirements specific to the ACOM2 the AZ family of parts communicates using a lower baud rate. Data transfers will not be as fast as those with an AS part. Note that the EPROM+ software provides a confirmation message to insure that communication has been established and valid data has been both transmitted and received.

## SELECTING THE PART

You may choose from any of the listed HC08/908 parts in the device selection table. The only difference is the amount of EEPROM contained in the device. All devices allow you to access the entire 64K address space for both EEPROM and RAM.

## CONNECTING THE ACOM2 ADAPTER TO THE 68HC08 TARGET PROCESSOR

Specific connections to the HC08 package must exist in order for the processor to enter monitor mode. Specific pins must be set to predefined voltage levels plus the processor clock must be running at 4.9152 MHZ for AS parts or 2.0000 MHZ for AZ parts. (Reference the connection diagrams at the end of this document.) The ACOM2 adapter is capable of providing all of the necessary signal levels to allow entry into monitor mode. **EXAMPLE:** To configure the MC68HC08AS32 the following levels must be applied to the device pins (52 pin PLCC package): PTC0 (#4 - +5V), PTC1 (#5 - GND), PTC3 (#7 - GND), IRQ (#9 - 9V), Vdd (#26 - +5V), Vss (#25 - GND). The ACOM2 adapter may be used to supply the +5V and GND levels. Specific ACOM2 signals must be connected to these device pins: (ACOM2 9VG pin - device pin #9 IRQ), (ACOM2 RCV pin - device pin #27 PTA0), (ACOM2 CLK - device pin #3 OSC1), ACOM2 RST - device pin #10 RST), (ACOM2 +5 - device pin #26 Vdd), ACOM2 GND - device pin #25 Vss). **NOTE:** Device pins #4 (+5), #5 (GND), and #7 (GND) must be at the proper voltage levels. These connections may be obtained from the ACOM2 +5 and GND pins or any +5 and GND connections on the target board. **NOTE:** It may be necessary to disconnect a processor pin or pins from the target circuit board to allow the proper voltage level to be applied. This is due to interference from existing circuitry on the target board. If you are unsuccessful in establishing communications with the target processor, use a volt meter to insure that each pin on the processor is indeed at the correct voltage level. You may also use the Andromeda Research Logic/Test Probe (#LP-1) to analyze a processor pin for drive capability or to determine the preexisting logic level before a probe is connected. Be sure to reconnect the pin(s) after you have finished working on the target assembly.

## ESTABLISHING COMMUNICATIONS

Before communications can be established, set the ACOM2 6 position dip switch as follows: SW1 ON (adapter to HC08 mode), SW2 OFF, SW3 (ON for AS parts/OFF for AZ parts), SW4 OFF, SW5 ON (9VG pin at 9 volts), SW6 OFF. Now set the adapter power switch to ON. The LED marked PWR will light indicating that the adapter and target processor are active. Press “Z” to access the DEVICE OPTIONS function. You are presented with three options: 1 - COMMUNICATE (EEPROM ONLY), 2 - COMMUNICATE (MONITOR 64K) AND 3 - COMMUNICATE (MON W/EEPROM). **NOTE:** You may also choose “O” which selects three additional options: 1 - EDIT SECURITY STRING, 2 - RUN USER PROGRAM and 3 - SET READ/PRGM CONFIRMATION.

The three primary selections have a common method by which communication is established. The sequence of steps follows for OPTION 1 - COMMUNICATE (EEPROM ONLY): Press "1" - The EPROM+ software issues a hardware reset to the target via the reset line then sends the 8 byte security string. Following this, the software attempts to write a byte into the internal RAM of the processor. While this occurs, you will see the message "ATTEMPTING COMMUNICATION...WAIT!". The software attempts several times to write data into the device and then read the data back. If data is successfully written and read from the device, then you will see the message "*COMMUNICATION CONFIRMED*". Once the "*COMMUNICATION CONFIRMED*" message is displayed the EPROM+ software has verified that communication can occur via the processor monitor mode.

## COMMUNICATION ERRORS

If communication cannot be established with the processor the software will display "WARNING! PROCESSOR NOT RESPONDING". This message indicates that the target processor has not issued the proper response to the initial communication attempt. The monitor mode protocol includes a character echo meaning that any character sent by the EPROM+ software will be echoed by the target system. If the software does not see the echoed character the PROCESSOR NOT RESPONDING message will be displayed. If this error occurs all connections, settings and voltage levels must be checked as the processor appears unresponsive to the EPROM+ software. The second possible error is "COMMUNICATION FAILED". This error is displayed if the processor responds (echoes characters) but the software cannot write and read data into the internal processor RAM. This error is caused by a processor where the monitor memory read/write capability has been disabled for security reasons. This is uncommon but possible. The third possible error is "MONITOR ENTRY FAILED!". This error is displayed if the processor does not send a "break" character (ten zero bits) after the SECURITY STRING has been sent. (See EDIT SECURITY STRING).

## COMMUNICATION CONFIRMED

If communication has been confirmed, the communication procedure sequence will differ depending on the selected option.

**OPTION 1 - COMMUNICATE (EEPROM ONLY)**

After the communication confirmed message you will see "UPLOADING EEPROM ACCESS PROGRAM..WAIT!". A progress counter is displayed below the message as a special program is uploaded into the RAM of the target prrocessor. After the program is uploaded you will see *BUFFER UPLOAD COMPLETE *. This program contains the algorithms which allow the reprogramming of the EEPROM area in the target processor. Once the program is uploaded, you may use any of the EPROM+ software commands to work with the EEPROM area. **NOTE:** The EEPROM area is remapped to appear as a single block which originates at 0 and ends at the address which corresponds to the last byte. **EXAMPLE:** The 68HC08AS32 has a single EEPROM block of 512 bytes. This block exists in the 64K address space between $800 and $9FF. The remapping feature allows you to work with the block of EEPROM as if it were a single memory device of 512 bytes ($0 to $1FF) without regard to the offset imposed by the processor memory map. If you wish to work with the actual physical device addresses, you may choose OPTION 2 or 3 (see below). **NOTE:** Some members of the HC08/908 family have two 512 byte blocks ($600-$7FF and $800 to $9FF) of EEPROM. These blocks are remapped to appear as a single block of 1024 bytes beginning at $0 and ending at $3FF ($0-$3FF -> $600-$9FF).

**PROGRAMMING SPEED** - The EEPROM programming algorithms are accessed via a monitor function called RUN PROGRAM. This function is somewhat slow to access the algorithms which results in a noticible programmming time for the entire EEPROM area. To reduce programming time you may use the buffer editor "W" (WRITE) command to change only the areas within the block you require. If you encounter programming errors, instruct the system to program the same block again.

**OPTION 2 - COMMUNICATE (MONITOR 64K)**

This establishes communication with the target and then leaves the processor in monitor mode. No EEPROM programming algorithms are uploaded. With this option the target is mapped as the entire 64K address space including all I/O, RAM and ROM. You may read any address within the 64K space, however you may only write RAM ($0050 to $044F) as this is the only command supported by the monitor to change internal memory. EEPROM, ROM or the programmable flash memory cannot be changed. You may also write data to any I/O address.

**OPTION 3 - COMMUNICATE (MON W/EEPROM)**

This option is identical to OPTION 2 except the EEPROM programming algorithms are uploaded. This allows you to work with the EEPROM while the memory blocks remain addressed at their actual offsets in the processor memory map. **NOTE:** When this option is active you must use the buffer editor "W" (WRITE) command and the "Z" (ZONE READ) command to read and program the EEPROM. Please familiarize yourself with these editor commands before attempting to work directly with the processor memory mapped blocks. Using any other commands will result in very long device accesses as the software will begin reading or programming the entire 64K address space. **NOTE:** The EEPROM algorithms are loaded into the target RAM between addreesses $200 and $2FF. If you write to this memory area the EEPROM routines will cease to function.

## ADDITIONAL OPTIONS

The EPROM+ software provides additional options which may be accessed by pressing "O" at the SELECT OPTION prompt. You may choose from three additional functions.

**1 - EDIT SECURITY STRING**

The SECURITY STRING consists of 8 bytes of data programmed into the target processor. Before the target processor will enable access to internal EEPROM or ROM, the EPROM+ software must first send a string of 8 bytes which matches the bytes programmed into the target. If the bytes do not match, monitor mode entry will be allowed but the EEPROM and ROM memory areas will not be visible. The EPROM+ software is initially set to send 8 bytes of $FF to the target. If the security string has not been programmed to a specific set of values, this will allow full memory access using the monitor. You have the option to change the security string sent to the target processor. This is accomplished using the EDIT SECURITY STRING option (Press "Z" then "O" then "1"). The system will display the existing security string as two groups of four FF characters. To change the string enter two groups of four valid hex characters with a space between the groups and press ENTER. The security bytes are identified by the yellow digits above each set of two. **NOTE:** The new security string will remain until the program terminates or you again change their values. The changes are not saved. **NOTE:** There is no published method for bypassing the SECURITY STRING. If you are attempting to read or change a device with a valid security string it will not be possible as the EEPROM area will be disabled.

**2 - RUN USER PROGRAM**

This option allows you to run a program you have uploaded into the RAM of the target processor. It uses the monitor RUN PROGRAM function to pass control to any program with a known starting address. To use this function it is assumed that you have the knowledge and skill to create an assembly language or binary program. You may set the origin of your program to be anywhere you wish as long as it resides within the RAM area of the target processor. Once your program is created, use the EPROM+ software to load it into the buffer at the address which matches the starting address in the target processor. The EPROM+ system supports automatic conversion of Motorola S-RECORD files so this is a convenient way to create your program using existing tools.

Once the program is loaded into the system buffer establish communication using OPTION 2. Once communication is confirmed use the "W" (WRITE) command to transfer the program from the buffer to the target processor RAM area.

From the START UP OPTIONS menu press "O" then "2". Enter the starting address for your program and press ENTER. Your program will begin to execute. **NOTE:** The only way to regain control after your program has started executing is to reset the target and reestablish communication. If you wish to view the data or results from you program, have your program write them to known memory addresses and then view the results after communication has been reestablished. Reestablishing communication does not alter the target RAM.

**3 - SET READ/PRGM CONFIRMATION**

This option allows you to change the data confirmation setting used by the EPROM+ software. To address occasional inconsistent communication issues which may occur while using MONITOR MODE, an additional layer of data confirmation is employed. If **CONFIRMATION MODE** is **ON** (default setting except for AZ parts), the EPROM+ reading algorithm will perform multiple data accesses of a memory location to confirm that the same data is returned each time. Only after good data has been confirmed is the data placed into the buffer. Programming operations are likewise confirmed for valid data by performing a read after each programming operation. If the desired data was not programmed correctly the operation is repeated. **NOTE:** CONFIRMATION MODE permits a very high level of confidence that the returned information is correct however to guarantee a perfect read of data from the device review the **MANUAL DATA VALIDATION** section below. If you wish to reduce the time required for reading and programming you may disable CONFIRMATION MODE. To turn CONFIRMATION MODE off press "Z" then "O" then "3". The current setting is displayed. To change the setting press "C". Pressing "C" is a toggle function. Once the desired setting is selected press the ESC key to exit.

**MANUAL DATA VALIDATION**

Although CONFIRMATION MODE normally results in the return of accurate data from the HC08/908 memory you may wish to use the following procedures to guarantee that the data is indeed valid.

**METHOD 1 (EEPROM AREA)** - Use COMMAND 3 (read device into buffer) followed by COMMAND 8 (compare device with buffer). Press 3 then Y (data will be read into buffer). Press 8 then Y (data in buffer will be compared with data in device). The system should indicate 0 errors when the comparison completes. If there are any errors perform the operations again until a 0 error result is obtained. 0 errors means that the data read from the device exactly matches the data in the buffer.

**METHOD 2 (EEPROM AREA or any 256 byte data block)** - Enter the buffer editor (Press 5). Use the ZONE READ command "Z" to read any 256 byte block of memory into the buffer at the address of your choice. Once the data has been read, use the "INSPECT" command with the compare option to examine any differences between the contents of the buffer and what is contained in the device. **EXAMPLE:** Press I then 0 then <space bar> then 0 then ENTER. This will access 256 bytes of data in the device at address 0 and then display any differences with the buffer data as reverse video blocks with the non-matching data.

# ACOM2 PROBE CONNECTIONS FOR MOTOROLA MICROCONTROLLERS

The following illustrations indicate which connections are necessary to allow the ACOM2 adapter to successfully communicate with the listed family member. Both the ACOM2 signal name and the probe color (#SMP8 or #PPS8) are shown. Packages were selected to illustrate the most common devices, however other parts are supported. In order to connect a microcontroller not shown, locate the part data sheet and reference the identical or corresponding pins. Attach the required ACOM2 signal to these pins and proceed according the the instructions in the applicable section of this document (68HC11, 68HC05 or 68HC08).

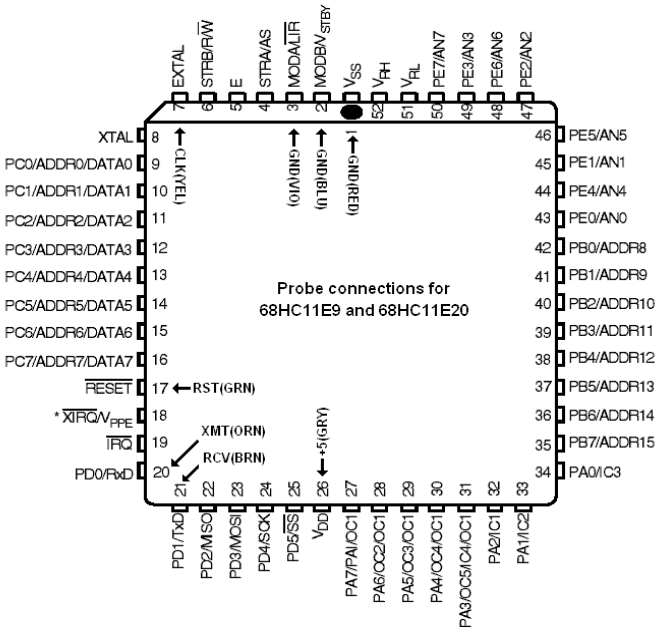
**IMPORTANT NOTE 1:** The ACOM2 adapter is designed with high current drivers which in most cases allow the attached microcontroller to be read and programmed in-circuit. If, however, you are not successful, you must determine which microcontroller pin is unable to be driven by the ACOM2 and disconnect (isolate) that pin from the circuit or module assembly. This can be done by carefully heating the pin with a low wattage soldering iron and using a small, sharp instrument to carefully lift the pin once the solder has melted. Once the pin has been lifted (isolated from the underlying board) connect the appropriate probe.

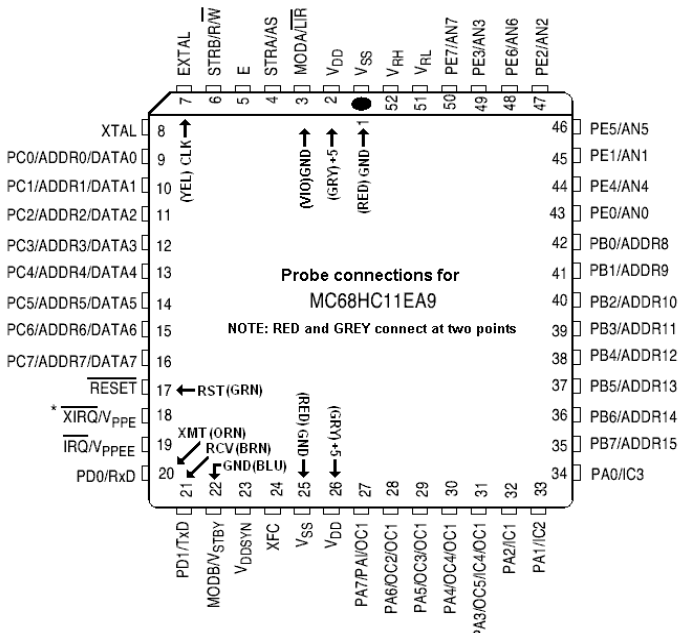
**IMPORTANT NOTE 2 (HC11 family):** To establish communication with the an HC11 family member both MODE (MODA and MODB) pins must be at a logic 0 (ground) state. This is accomplished using the BLUE and VIOLET probes. If all probes are connected and the ACOM2 power switch is set to ON the LED on the adapter should light. If the LED does not light then one of the MODE pins must be lifted as it is connected directly to the +5 volt module supply (GRY probe). This shorts out the power to the module which causes the programmer to current limit and the LED not to light. Turn the adapter switch OFF and remove one MOD probe (BLU or VIO) at a time until the switch can be set to ON with the LED lit. The probe color which causes the LED to remain OFF when connected is the pin which must be lifted. NOTE: You may also use the Andromeda Research Logic/Test Probe (#LP-1) to test a pin.

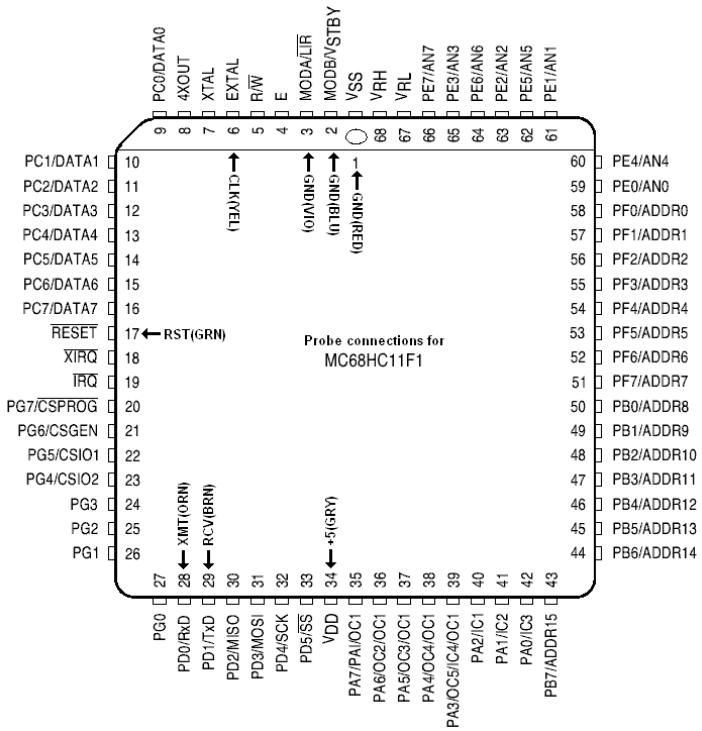
**OTHER PINS WHICH MAY CAUSE PROBLEMS:** HC11 family (RST, RCV, XMT), HC05 family (9VG, RST, RCV, XMT), HC08/908 family (9VG, RST, RCV) The HC05, 08/908 parts require that the IRQ pin voltage be at +9 volts. This is sourced from the 9VG (VIO) probe. If communication cannot be established measure the voltage between this pin and GND to confirm the correct value (9V). If the value is below 8 volts the pin must be lifted.

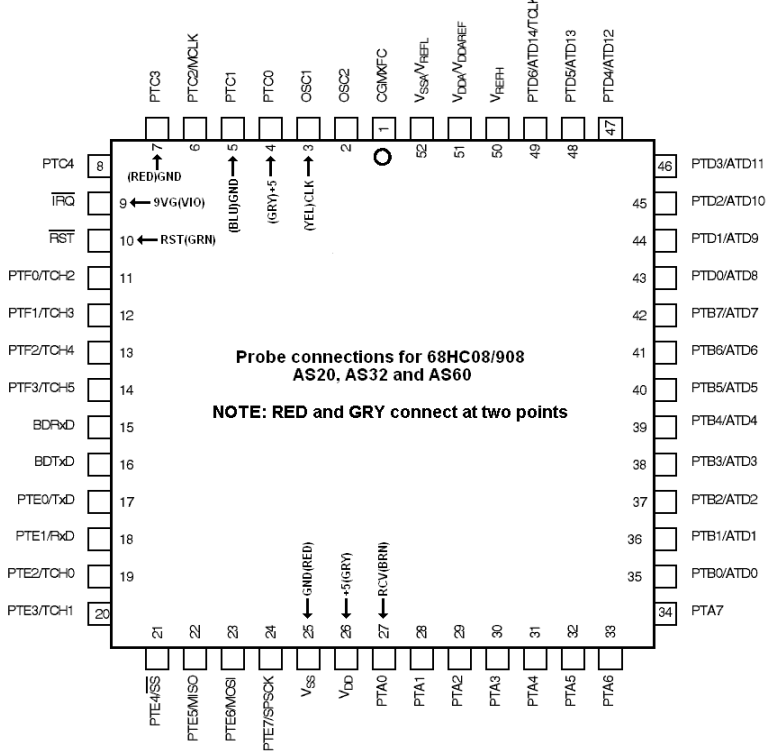
**IMPORTANT NOTE 3:** You should never lift a power supply pin (Vdd or Vss) on any microcontroller. These pins must remain connected as they supply current to other pins and use the module power supply by-pass capacitors for power stability. Also you only need to connect +5 and GND to one set of Vdd and Vss pins.

**IMPORTANT NOTE 4:** If multiple connections of a single voltage probe are required, attach an extension probe to the primary signal probe for the connection(s).



# DIAGRAMS
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